What is claimed is:

1. A semiconductor device, comprising:

pads formed on a semiconductor chip;

conductive sections connected to said pads, respectively;

conductive bumps on surfaces of said conductive sections; and

an insulating film covering said semiconductor chip other than the surfaces of said conductive sections, and

wherein said insulating film including a stress buffering layer in a lateral direction of said conductive sections to relax a stress applied to said bumps.

2. The semiconductor device according to claim 1, wherein said insulating film covers said semiconductor chip other than the surfaces of said conductive sections without including a printed circuit board.

3. The semiconductor device according to claim 1, wherein said stress buffering layer has an elastic modulus in a range of 0.01 to 8 Gpa.

4. The semiconductor device according to claim 1, wherein said stress buffering layer is formed of material comprising at least one selected from a group

consisting of epoxy-based resin, silicon-based resin, polyimide-based resin, polyolefin-based resin, cyanate-ester-based resin, phenol-based resin, naphthalene-based resin, and fluorine-based resin.

5. The semiconductor device according to claim 1, wherein said stress buffering layer includes a plurality of buffering layers, each of which is formed of material comprising at least one selected from a group consisting of epoxy-based resin, silicon-based resin, polyimide-based resin, polyolefin-based resin, cyanate-ester-based resin, phenol-based resin, naphthalene-based resin, and fluorine-based resin.

6. The semiconductor device according to claim 5, wherein each of said conductive sections includes a plurality of portions respectively corresponding to said plurality of buffering layers.

7. The semiconductor device according to claim 1, wherein said conductive section is connected to said pad via a wiring pattern provided on said semiconductor chip via a first insulting film of said insulating film.

8. The semiconductor device according to claim 7, wherein said wiring pattern is formed of copper (Cu).

9. The semiconductor device according to claim 7, wherein said wiring pattern extends to adjust a pitch between said conductive bump and another conductive bump.

10. The semiconductor device according to claim 7, wherein said first insulating film includes:

a passivation film covering said semiconductor chip other than said pads; and

a second insulating film formed on said passivation film.

11. The semiconductor device according to claim 10, wherein said second insulating film has a pyrolysis temperature of 200℃ or more.

12. The semiconductor device according to claim 10, wherein said second insulating film is formed of a photosensitive material.

13. A method of manufacturing a semiconductor device, comprising:

(a) providing a semiconductor substrate formed on which pads are formed and on which a first insulating film are formed to have openings, said pads being exposed by said openings;

(b) forming wiring patterns to extend on said

first insulating film and to be respectively connected to said pads;

(c) forming a stress buffering layer on said wiring patterns and said first insulating film, said buffering layer including conductive sections respectively connected to said wiring patterns and a buffering and insulating layer formed to surround said conductive sections on lateral sides thereof; and

(d) forming conductive bumps on surfaces of said conductive sections.

14. The method according to claim 13, further comprising:

(e) separating said semiconductor substrate into semiconductor chips.

15. The method according to claim 13, wherein said (a) providing includes:

forming said pads;

forming a passivation film on said semiconductor substrate to have openings in said pads; and

forming a second insulating film formed on said passivation film.

16. The method according to claim 15, wherein said second insulating film is formed of material

having a pyrolysis temperature of 200℃ or more.

17. The method according to claim 15, wherein said second insulating film is formed of a photosensitive material.

18. The method according to claim 13, wherein said (b) forming includes:

carrying out electrolysis plating to produce a conductive layer; and

patterning said conductive layer to produce said wiring patterns.

19. The method according to claim 13, wherein said (c) forming includes:

connecting said conductive sections to said wiring patterns;

forming said buffering and insulating layer to cover said first insulating film and said wiring patterns; and

polishing said buffering and insulating layer and said conductive sections to expose said surfaces of said conductive sections.

20. The method according to claim 19, wherein said buffering and insulating layer has an elastic modulus in a range of 0.01 to 8 Gpa.

21. The method according to claim 19, wherein said buffering and insulating layer is formed of material comprising at least one selected from a group consisting of epoxy-based resin, silicon-based resin, polyimide-based resin, polyolefin-based resin, cyanate-ester-based resin, phenol-based resin, naphthalene-based resin, and fluorine-based resin.

22. The method according to claim 13, wherein said buffering and insulating film includes first and second buffering and insulating films, and each of said conductive sections includes first and second conductive sections, and

said (c) forming includes:

connecting said first conductive sections to said wiring patterns;

forming said first buffering and insulating layer to cover said first insulating film and said wiring patterns;

polishing said first buffering and insulating layer and said first conductive sections to expose said surfaces of said first conductive sections;

connecting said second conductive sections to said first conductive sections;

forming said second buffering and insulating layer to cover said first buffering and insulating layer and said second conductive sections; and

polishing said second buffering and insulating layer and said second conductive sections to expose said surfaces of said second conductive sections.

23. The method according to claim 22, wherein each of said first and second buffering and insulating layers has an elastic modulus in a range of 0.01 to 8 Gpa.

24. The method according to claim 22, wherein each of said first and second buffering and insulating layers is formed of material comprising at least one selected from a group consisting of epoxy-based resin, silicon-based resin, polyimide-based resin, polyolefin-based resin, cyanate-ester-based resin, phenol-based resin, naphthalene-based resin, and fluorine-based resin.